HOLT INC.
INTEGRATED CIRCUITS

HI-8382, HI-8383

ARINC 429 Differential Line Driver

September 2011

GENERAL DESCRIPTION

The HI-8382 and HI-8383 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-8382 to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

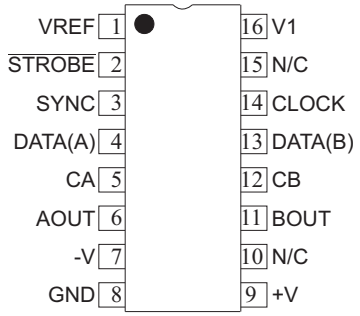
The differential outputs of the HI-8382 are independently programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. The HI-8382 has on-chip Zener diodes in series with a fuse to each differential output protecting the ARINC bus from an overvoltage failure. The outputs each have a series resistance of 37.5 ohms. The HI-8383 is identical to the HI-8382 except that the series resistors are 13 ohms and the overvoltage protection circuitry has been eliminated.

The updated HI-318X and HI-8585 ARINC 429 line drivers are recommended for all new designs where logic signals must be converted to ARINC 429 levels such as a user ASIC, the HI-3282 or HI-8282A ARINC 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC interface device. Holt products are readily available for both industrial and military applications. Please contact the Holt Sales Department for additional information, including data sheets for any of the Holt products mentioned above.

FEATURES

- Low power CMOS
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Operates at data rates up to 100 Kbits
- Overvoltage protection
- Industrial and extended temperature ranges
- DSCC SMD part number

PIN CONFIGURATION (Top View)

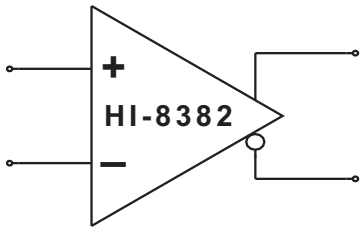


HI-8382C / CT / CM-01 / CM-03
SMD # 5962-8687901EA

16 - PIN CERAMIC SIDE-BRAZED DIP

(See Page 6 for additional package pin configurations)

FUNCTION



ARINC 429 DIFFERENTIAL LINE DRIVER

TRUTH TABLE

SYNC	CLOCK	DATA(A)	DATA(B)	AOUT	BOUT	COMMENTS
X	L	X	X	0V	0V	NULL
L	X	X	X	0V	0V	NULL
H	H	L	L	0V	0V	NULL
H	H	L	H	-VREF	+VREF	LOW
H	H	H	L	+VREF	-VREF	HIGH
H	H	H	H	0V	0V	NULL

FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input. Each logic input, including the power enable ($\overline{\text{STROBE}}$) input, are TTL/CMOS compatible. Besides reducing chip current drain, $\overline{\text{STROBE}}$ also floats each output. However the overvoltage fuses and diodes of the HI-8382 are not switched out.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-8382; typically +15V, -15V and +5V. The chip also works with ±12V supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal $2V_{REF}$. If a value of V_{REF} other than +5V is needed, a separate +5V power supply is required for pin V_1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, A_{OUT} will switch to the $+V_{REF}$ rail and B_{OUT} will switch to the $-V_{REF}$ rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to 0V (ARINC NULL state).

The driver output impedance, R_{OUT}, is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the C_A and C_B input pins. Typical values for high-speed operation (100KBPS) are $C_A = C_B = 75pF$ and for low-speed operation (12.5 to 14KBPS) $C_A = C_B = 500pF$.
The driver can be externally powered down by applying a logic high to the $\overline{\text{STROBE}}$ input pin. If this feature is not being used, the pin should be tied to ground.

The C_A and C_B pins are inputs to unity gain amplifiers. Therefore they must be allowed to swing to -5V. Provision to switch capacitors must be done with analog switches that allow voltages below their ground.

Both ARINC outputs of the HI-8382 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125µs).

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V_1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.

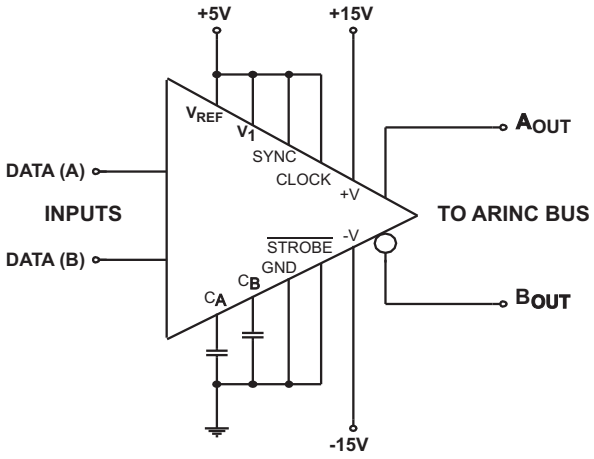


Figure 1. **ARINC 429 BUS APPLICATION**

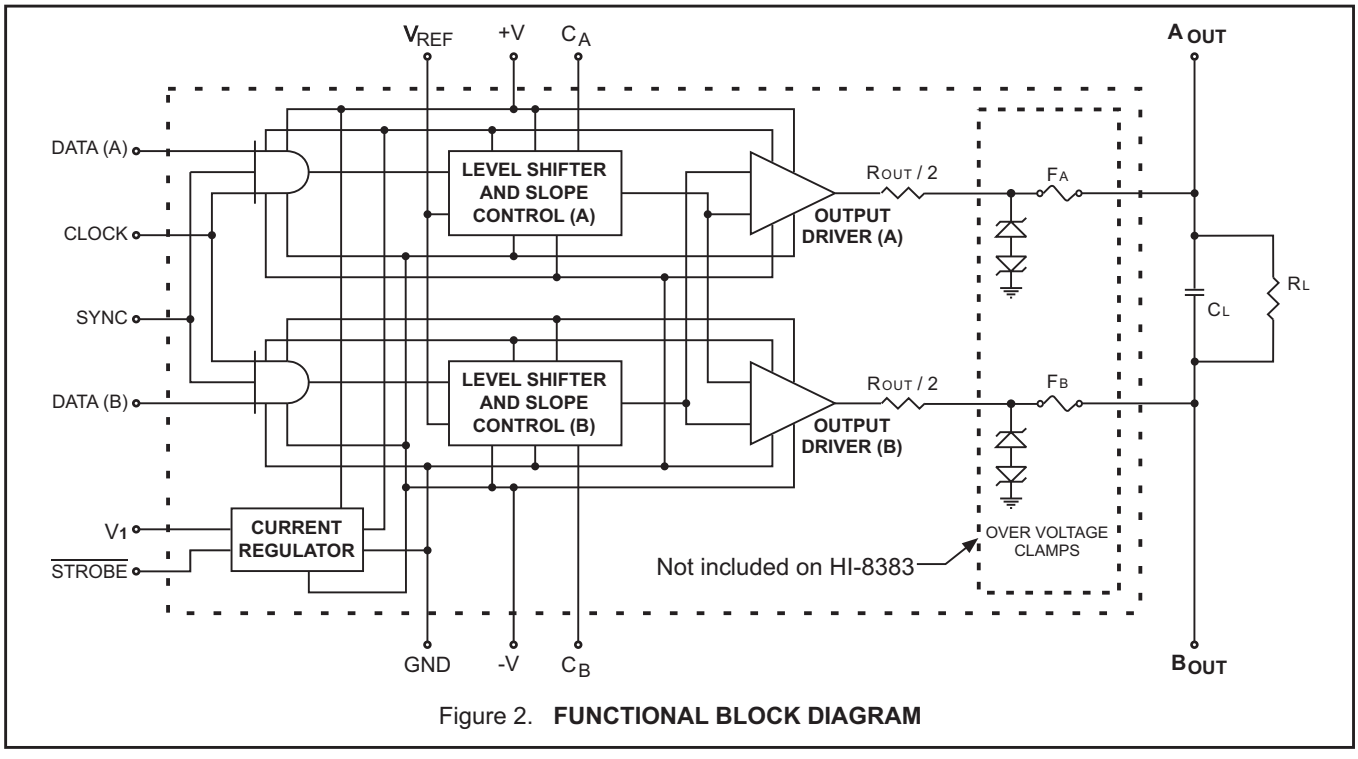


Figure 2. **FUNCTIONAL BLOCK DIAGRAM**

PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
V_{REF}	POWER	THE REFERENCE VOLTAGE USED TO DETERMINE THE OUTPUT VOLTAGE SWING
$\overline{STROBE}$	INPUT	A LOGIC HIGH ON THIS INPUT PLACES THE DRIVER IN POWER DOWN MODE
SYNC	INPUT	SYNCHRONIZES DATA INPUTS
DATA (A)	INPUT	DATA INPUT TERMINAL A
C_A	INPUT	CONNECTION FOR DATA (A) SLEW-RATE CAPACITOR
A_{OUT}	OUTPUT	ARINC OUTPUT TERMINAL A
-V	POWER	-12V to -15V
GND	POWER	0.0V
+V	POWER	+12V to +15V
B_{OUT}	OUTPUT	ARINC OUTPUT TERMINAL B
C_B	INPUT	CONNECTION FOR DATA (B) SLEW-RATE CAPACITOR
DATA (B)	INPUT	DATA INPUT TERMINAL B
CLOCK	INPUT	SYNCHRONIZES DATA INPUTS
V_1	POWER	+5V ±5%

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	V_{DIF}	Voltage between +V and -V terminals		40	V
Supply Voltage	+V -V V_1		+10.8 to +16.5 -10.8 to -16.5 +5 ±5%	 +7	V V V
Voltage Reference	V_{REF}	For ARINC 429 For Applications other than ARINC	+5 ±5% 0 to 6	6 6	V V
Input Voltage Range	V_{IN}			$\geq$ GND -0.3 $\leq$ V1 +0.3	V V
Output Short-Circuit Duration		See Note: 1			
Output Overvoltage Protection		See Note: 2			
Operating Temperature Range	T_A	Extended Industrial	-55 to +125 -40 to +85		°C °C
Storage Temperature Range	T_{STG}	Ceramic & Plastic	-65 to +150		°C
Lead Temperature		Soldering, 10 seconds		+275	°C
Junction Temperature	T_J			+175	°C
Power Dissipation	P_D	16-Pin Ceramic DIP See Note: 3 28-Pin Ceramic LCC See Note: 3 28-Pin Plastic PLCC See Note: 3 32-Pin CERQUAD See Note: 3		1.725 1.120 2.143 1.725	W W W W
Thermal Resistance, (Junction-to-Ambient)	$Ø_{JA}$	16-Pin Ceramic DIP 28-Pin Ceramic LCC 28-Pin Plastic PLCC 32-Pin CERQUAD		86.5 133.7 70.0 86.5	°C/W °C/W °C/W °C/W

Note 1. Heatsinking may be required for Output Short Circuit at +125°C and for 100KBPS at +125°C.
Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-8382 only)
Note 3. Derate above +25°C, 11.5mW/°C for 16-PIN DIP and 32-PIN CERQUAD, 7.5 mW/°C for 28-PIN LCC, 14.2 mW/°C for 28-PIN PLCC

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_1 = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Current +V (Operating)	I_{CCOP} (+V)	No Load (0 - 100KBPS)			+11	mA
Supply Current -V (Operating)	I_{CCOP} (-V)	No Load (0 - 100KBPS)	-11			mA
Supply Current V_1 (Operating)	I_{CCOP} (V_1)	No Load (0 - 100KBPS)			500	µA
Supply Current V_{REF} (Operating)	I_{CCOP} (V_{REF})	No Load (0 - 100KBPS)			500	µA
Supply Current +V (Power Down)	I_{CCPD} (+V)	STROBE = HIGH			475	uA
Supply Current -V (Power Down)	I_{CCPD} (-V)	STROBE = HIGH	-475			uA
Supply Current +V (During Short Circuit Test)	I_{SC} (+V)	Short to Ground (See Note: 1)			150	mA
Supply Current -V (During Short Circuit Test)	I_{SC} (-V)	Short to Ground (See Note: 1)	-150			mA
Output Short Circuit Current (Output High)	I_{OHSC}	Short to Ground V_{MIN}=0 (See Note: 2)			-80	mA
Output Short Circuit Current (Output Low)	I_{OLSC}	Short to Ground V_{MIN}=0 (See Note: 2)	+80			mA
Input Current (Input High)	I_{IH}				1.0	µA
Input Current (Input Low)	I_{IL}				-1.0	µA
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.5	V
Output Voltage High (Output to Ground)	V_{OH}	No Load (0 -100KBPS)	$+V_{REF}$ -.25		$+V_{REF}$ +.25	V
Output Voltage Low (Output to Ground)	V_{OL}	No Load (0 -100KBPS)	$-V_{REF}$ -.25		$-V_{REF}$ +.25	V
Output Voltage Null	V_{NULL}	No Load (0-100KBPS)	-250		+250	mV
Input Capacitance	C_{IN}	See Note 1		15		pF

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.
Note 2. Interchangeability of force and sense is acceptable.

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V_1 = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Rise Time (A_{OUT}, B_{OUT})	t_R	C_A = C_B = 75pF See Figure 3.	1.0		2.0	µs
Fall Time (A_{OUT}, B_{OUT})	t_F	C_A = C_B = 75pF See Figure 3.	1.0		2.0	µs
Propagtion Delay Input to Output	t_{PLH}	C_A = C_B = 75pF See Figure 3.			3.0	µs
Propagtion Delay Input to Output	t_{PHL}	C_A = C_B = 75pF See Figure 3.			3.0	µs

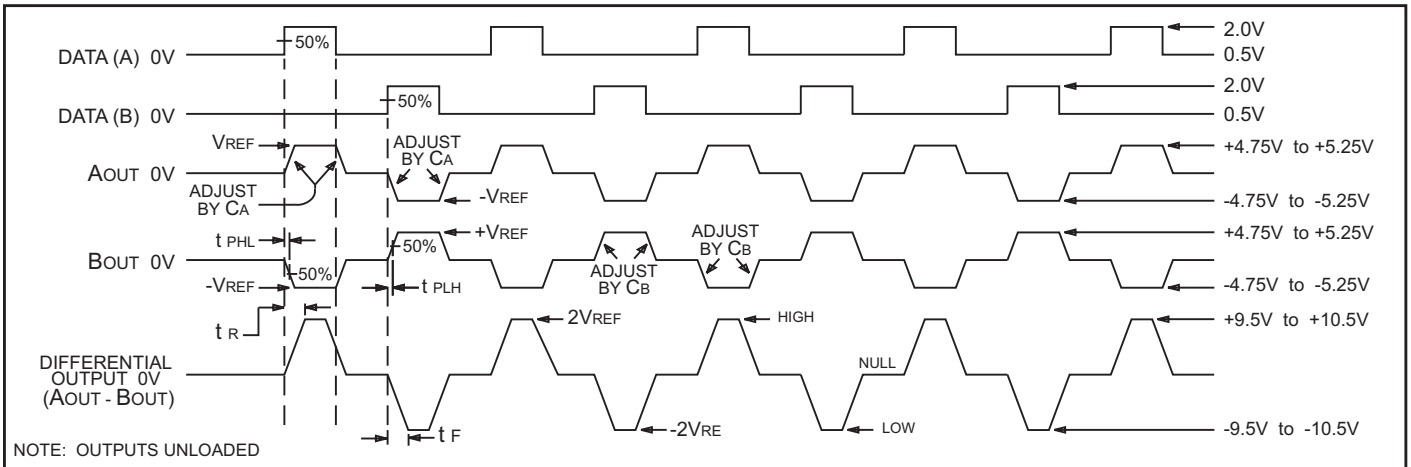


Figure 3. **SWITCHING WAVEFORMS**

HI-8382 PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD [7]

PACKAGE STYLE [1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) [2]			JUNCTION TEMP, Tj (°C)		
		Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
28 Lead PLCC	Low Speed [3]	17.6	17.2	17.0	48	107	142
	High Speed [4]	25.4	24.5	24.2	56	110	150
16 Lead Ceramic SB DIP	Low Speed	17.9	17.4	17.1	41	103	145
	High Speed	25.8	24.8	24.4	47	112	147

AOUT and BOUT Shorted To Ground [5, 6, 7]

PACKAGE STYLE [1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) [2]			JUNCTION TEMP, Tj (°C)		
		Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
28 Lead PLCC	Low Speed [3]	60.1	55.7	52.4	110	157	194
	High Speed [4]	63.1	56.3	52.3	100	150	182
16 Lead Ceramic SB DIP	Low Speed	62.1	56.2	53.0	90	145	180
	High Speed	64.0	56.2	52.2	86	144	176

Notes:

1. All data taken in still air on devices soldered to a single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. Similar results would be obtained with AOUT shorted to BOUT.
6. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
7. Data will vary depending on air flow and the method of heat sinking employed.

ORDERING INFORMATION

HI - 838x x x - xx (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	NOTES
Blank	-40°C to +85°C	I	No	
T	-55°C to +125°C	T	No	
M-01	-55°C to +125°C	M	Yes	(1)
M-03	-55°C to +125°C	DSCC	Yes	(1) & (2)

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH	NOTES
C	16 PIN CERAMIC SIDE BRAZED DIP (16C)	Gold	(3) & (1)
S	28 PIN CERAMIC LEADLESS CHIP CARRIER (28S)	Gold	(3) & (1)
U	32 PIN CERQUAD (32U) not available with 'M' flow	Tin/Lead Solder	

PART NUMBER	OUTPUT SERIES	
	RESISTANCE	FUSE
8382	37.5 Ohms	Yes
8383	13 Ohms	No

(1) Process Flows M and DSCC always have Tin/Lead (Sn/Pb) solder lead finish.
(2) DSCC SMD# 5962-8687901EA. Only available in "C" package with Sn/Pb solder lead finish.
(3) Gold terminal finish is Pb-Free, RoHS compliant.

HI - 838xJ x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

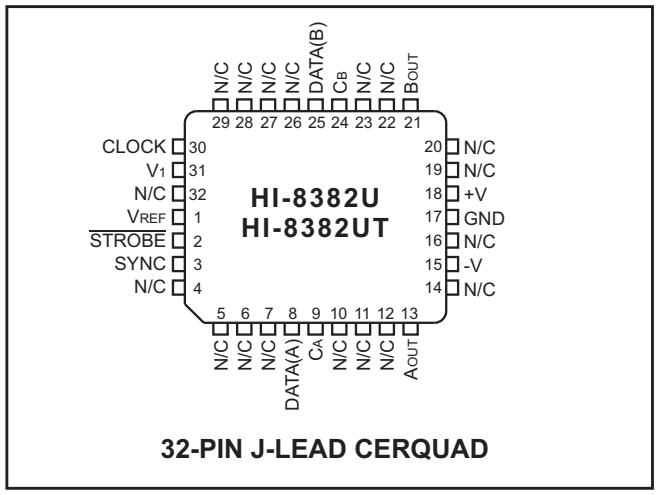
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
Blank	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION	OUTPUT SERIES	
		RESISTANCE	FUSE
8382J	28 PIN PLASTIC PLCC (28J) (1)	37.5 Ohms	Yes
8383J	28 PIN PLASTIC PLCC (28J) (1)	13 Ohms	No

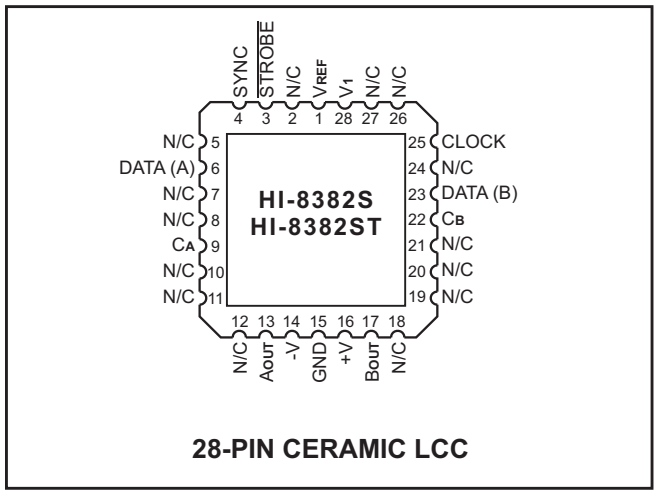
(1) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-3182PJxx and HI-3183PJxx are drop-in replacements for the older HI-8382Jxx and HI-8383Jxx respectively.

ADDITIONAL PIN CONFIGURATIONS

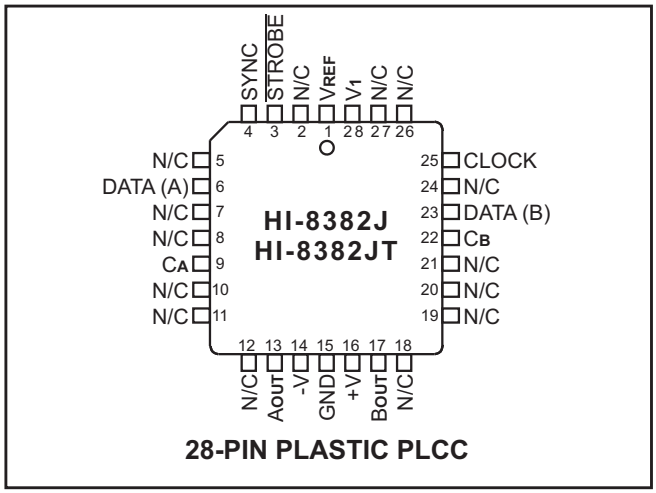
(See page 1 for the 16-pin Ceramic Side-Brazed DIP Package)



32-PIN J-LEAD CERQUAD



28-PIN CERAMIC LCC



28-PIN PLASTIC PLCC

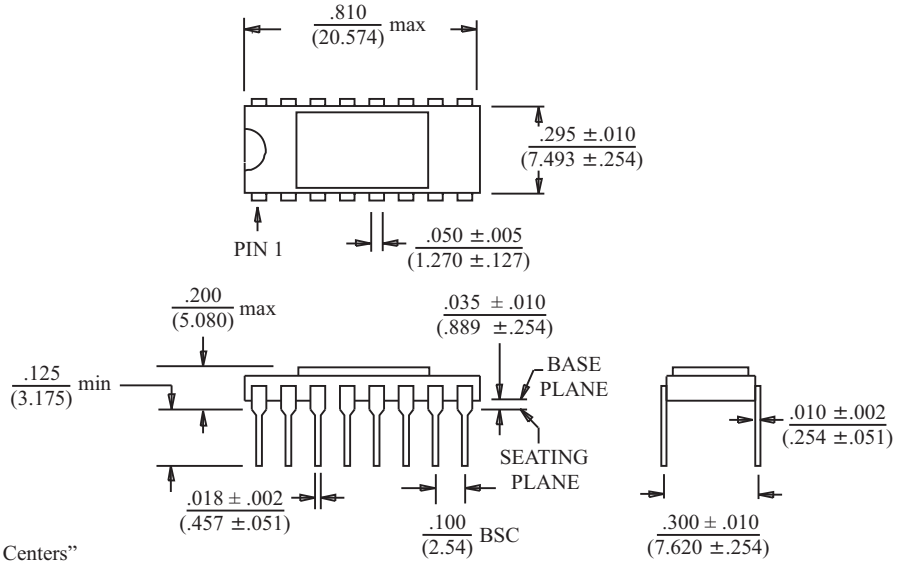
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8382	E	02/26/09	Clarified the temperature ranges, and Note (1) in the Ordering Information.
	F	09/16/11	Realigned pin names and numbers with package pin locations in Additional Pin Configuration drawings.

16-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 16C

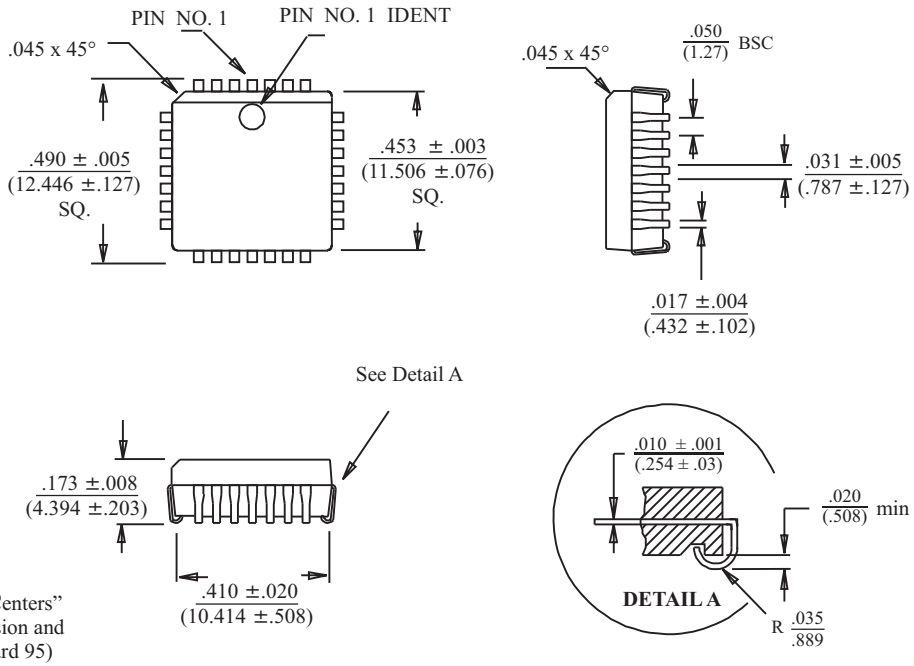


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

28-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 28J

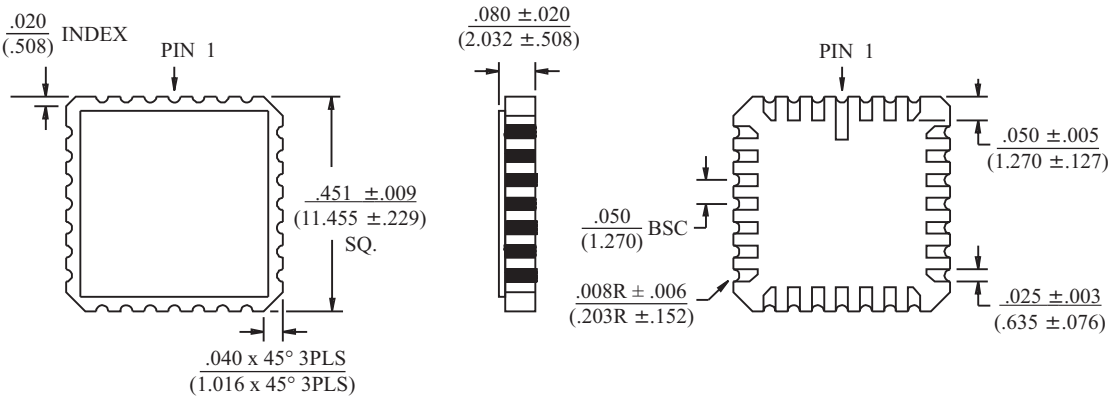


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

28-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 28S

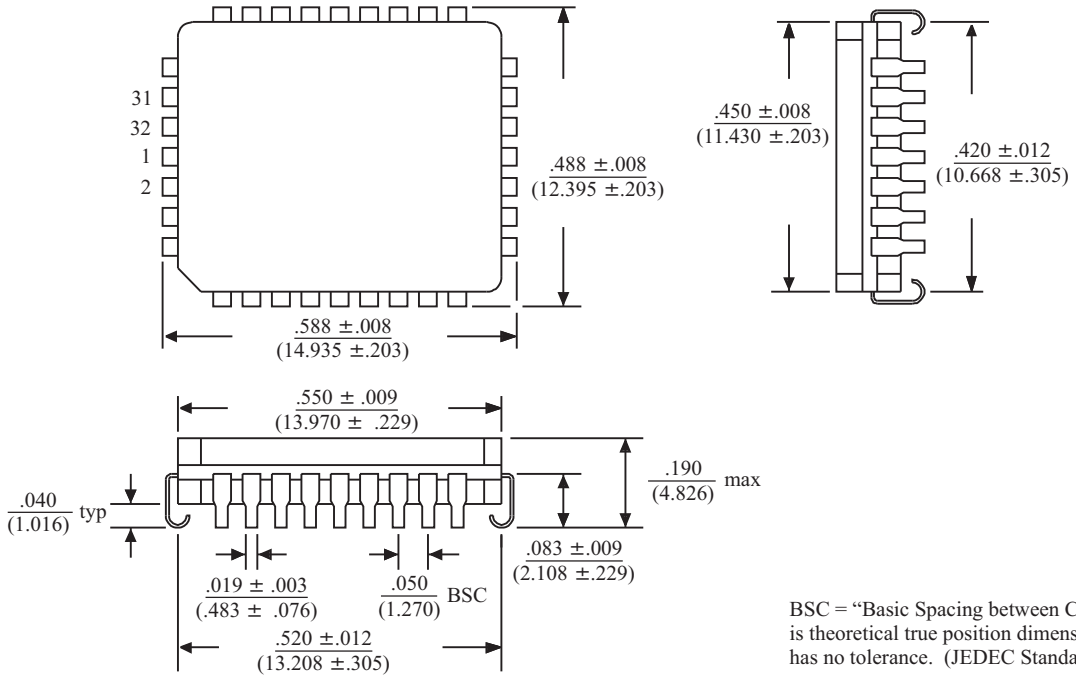


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 32U



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